

Access DB# 52970**SEARCH REQUEST FORM**
Scientific and Technical Information Center

Requester's Full Name: P. Laufer Examiner#: 73139 Date: 10/15/01
Art Unit: 2100 Phone Number: 306-4160 Serial Number: 09/871978
Mail Box and Bldg/Room Location: _____ Results Format Preferred (circle): Paper Disk E-mail

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Litigation
5,910,181

10-15-01 P12:08 IN

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	Type of search	Vendors and cost where applicable
Searcher: <u>A Green</u>	NA Sequence (#) _____	STN _____
Searcher Phone: <u>6-4767</u>	AA Sequence (#) _____	Dialog <u>1 min</u>
Searcher Location: <u>4B40</u>	Structure (#) _____	Questel/Orbit <u>6 min</u>
Date Searcher Picked Up: <u>10/15/01</u>	Bibliographic _____	Dr. Link _____
Date Completed: <u>10/15/01</u>	Litigation <input checked="" type="checkbox"/>	Lexis/Nexis <u>3 1/2</u>
Searcher Prep & Review Time: _____	Full Text _____	Sequence System _____
Clerical Prep Time: _____	Patent Family _____	WWW/Internet _____
Online Time: _____	Other _____	Other (specify) _____

Green, Shirelle

From: Laufer, Pinchus
Sent: Monday, October 15, 2001 11:41 AM
To: STIC-EIC2100
Subject: More litigation searches - CAN THESE BE PUT "NEXT"
Importance: High

Here are 2 more; CAN THESE BE DONE BEFORE THE 3?

(1) 09/821,371 which is a Reissue of US Patent 5,890,128 Inventors: Benjamin Diaz and M. Inez Genera

(2) 09/871,978 which is a Reissue of US Patent 5,910,181 Inventors: Makoto Hatakenaka et al.

Thank You,

Pinchus

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Computer Architecture, Software, & Electronic Commerce
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(703) 306-4160
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S1 1 PN="US 5910181"
?t sl/9

1/9/1
DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat
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14683804
Basic Patent (No,Kind,Date): DE 19755707 A1 19981008 <No. of Patents: 004
>

PATENT FAMILY:
CHINA (CN)

Patent (No,Kind,Date): CN 1195891 A 19981014
SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING SYNCHRONOUS
DYNAMIC RANDOM MEMORY CORE (English)
Patent Assignee: MITSUBISHI ELECTRIC CORP (JP)
Author (Inventor): HATAKENAKA MAKOTO (JP); YAMAZAKI AKIRA (JP);
TOMISHIMA SHIGEKI (JP)
Priority (No,Kind,Date): JP 9786600 A 19970404
Applic (No,Kind,Date): CN 97125547 A 19971212
IPC: * H01L-027/108; G01R-031/3183
Derwent WPI Acc No: * G 98-533087
Language of Document: Chinese

GERMANY (DE)

Patent (No,Kind,Date): DE 19755707 A1 19981008
INTEGRIERTE HALBLEITERSCHALTUNG MIT IN EINEM EINZELCHIP INTEGRIERTEN
SYNCHRONEN DRAM-KERN UND LOGIK-SCHALTKREIS SOWIE VERFAHREN ZUM
PRUEFEN DES SYNCHRONEN DRAM-KERNS Single semiconductor chip with
SDRAM core and integrated logic circuit (German)
Patent Assignee: MITSUBISHI ELECTRIC CORP (JP)
Author (Inventor): HATAKENAKA MAKOTO (JP); TOMISHIMA SHIGEKI (JP);
YAMAZAKI AKIRA (JP); YAMAGATA TADATO (JP)
Priority (No,Kind,Date): JP 9786600 A 19970404
Applic (No,Kind,Date): DE 19755707 A 19971215
IPC: * G11C-011/407
Derwent WPI Acc No: * G 98-533087; G 98-533087
Language of Document: German

GERMANY (DE)

Legal Status (No,Type,Date,Code,Text):
DE 19755707 P 19970404 DE AA PRIORITY (PATENT
APPLICATION) (PRIORITAET (PATENTANMELDUNG))
JP 9786600 A 19970404
DE 19755707 P 19971215 DE AE DOMESTIC APPLICATION (PATENT
APPLICATION) (INLANDSANMELDUNG
(PATENTANMELDUNG))
DE 19755707 A 19971215
DE 19755707 P 19981008 DE A1 LAYING OPEN FOR PUBLIC
INSPECTION (OFFENLEGUNG)
DE 19755707 P 19981008 DE OP8 REQUEST FOR EXAMINATION AS
TO PARAGRAPH 44 PATENT LAW (PRUEFUNGSANTRAG
GEM. PAR. 44 PATG. IST GESTELLT)

JAPAN (JP)

Patent (No,Kind,Date): JP 10283777 A2 19981023
SEMICONDUCTOR INTEGRATED CIRCUIT WHERE SDRAM CORE AND LOGIC CIRCUIT ARE
MIXEDLY MOUNTED ON SINGLE CHIP AND TESTING METHOD OF THE SDRAM CORE
(English)
Patent Assignee: MITSUBISHI ELECTRIC CORP

Author (Inventor): HATANAKA MAKOTO; YAMAZAKI AKIRA; TOMISHIMA SHIGEKI;
YAMAGATA NARIHITO
Priority (No,Kind,Date): JP 9786600 A 19970404
Applic (No,Kind,Date): JP 9786600 A 19970404
IPC: * G11C-011/407; G11C-011/401; G11C-029/00
Derwent WPI Acc No: * G 98-533087
Language of Document: Japanese

UNITED STATES OF AMERICA (US)

Patent (No,Kind,Date): US 5910181 A 19990608
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE COMPRISING SYNCHRONOUS DRAM
CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF
TESTING THE SYNCHRONOUS DRAM CORE (English)
Patent Assignee: MITSUBISHI ELECTRIC CORP (JP)
Author (Inventor): HATAKENAKA MAKOTO (JP); YAMAZAKI AKIRA (JP);
TOMISHIMA SHIGEKI (JP); YAMAGATA TADATO (JP)
Priority (No,Kind,Date): JP 9786600 A 19970404
Applic (No,Kind,Date): US 964236 A 19971104
National Class: * 714718000
IPC: * G06F-011/00
Derwent WPI Acc No: * G 98-533087
Language of Document: English

UNITED STATES OF AMERICA (US)

Legal Status (No,Type,Date,Code,Text):
US 5910181 P 19970404 US AA PRIORITY (PATENT)
JP 9786600 A 19970404
US 5910181 P 19971104 US AE APPLICATION DATA (PATENT)
(APPL. DATA (PATENT))
US 964236 A 19971104
US 5910181 P 19971104 US AS02 ASSIGNMENT OF ASSIGNOR'S
INTEREST
MITSUBISHI DENKI KABUSHIKI KAISHA 2-3,
MARUNOUCHI 2-CHOME, CHIYODA-KU TOKYO 100, ;
HATAKENAKA, MAKOTO : 19971020; YAMAZAKI,
AKIRA : 19971020; TOMISHIMA, SHIGEKI :
19971027; YAMAGATA, TADATO : 19971020
US 5910181 P 19990608 US A PATENT

Litigations - 5910181 - P. Laufer

?us5910181/pn

Term not in index/PN-CRXX : US5910181
Term not in index/PN-LITA : US5910181
Term not in index/PN-PAST : US5910181

LGST	1
CRXX	0
LITA	0
PAST	0

** SS 2 : Results 1

Search statement 3

?prt ss2 max 1

1/1 LGST (1/1) - (C) LEGSTAT
PN - US 5910181 [US5910181]
AP - US 964236/97 19971104 [1997US-0964236]
DT - US-P
ACT - 19971104 US/AE-A
APPLICATION DATA (PATENT)
{US 964236/97 19971104 [1997US-0964236]}
- 19971104 US/AS02
ASSIGNMENT OF ASSIGNOR'S INTEREST
MITSUBISHI DENKI KABUSHIKI KAISHA 2-3, MARUNOUCHI 2-CHOME, CHIYODA-KU
TOKYO 100, * HATAKENAKA, MAKOTO : 19971020; YAMAZAKI, AKIRA :
19971020; TOMISHIMA, SHIGEKI : 19971027; YAMAGATA, TADATO : 19971020
- 19990608 US/A
PATENT
UP - 2000-06

LEVEL 1 OF 1 PATENT

5,910,181

<=2> GET 1st DRAWING SHEET OF 15

Jun. 8, 1999

Semiconductor integrated circuit device comprising
synchronous DRAM core and logic circuit integrated into a
single chip and method of testing the synchronous DRAM core

CORE TERMS: pin, external, input, semiconductor, integrated, control signals,
synchronous, dynamic, clock, random access memory...

LEXIS-NEXIS
Library: PATENT
File: ALL

5,910,181 OR 5910181

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LEXIS-NEXIS
Library: PATENT
File: CASES

5,910,181 OR 5910181

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5,910,181 OR 5910181

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LEXIS-NEXIS
Library: PATENT
File: JNLS